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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): Berger, Alexander J.; Kretz, Frank E.
Assignee: Tru-Si Technologies, Inc.
Title: Alignment of Semiconductor Wafers And Other Articles
Serial No.: 09/905,218 Filing Date: July 13, 2001
Examiner: Not yet known Group Art Unit: Not yet known
Docket No.: M-11882 US

San Jose, California
August 14, 2001

COMMISSIONER FOR PATENTS
Washington, D.C. 20231

INFORMATION DISCLOSURE STATEMENT
UNDER 37 CFR § 1.97(b)

Dear Sir:

Pursuant to 37 C.F.R. § 1.56, § 1.97 and § 1.98, the documents listed on the accompanying form PTO-1449 are called to the attention of the Examiner for the above patent application. Copies of these documents are enclosed.

Citation of these documents shall not be construed as:

1. an admission that the documents are necessarily prior art with respect to the instant invention;
2. a representation that a search has been made, or
3. an admission that the information cited herein is, or is considered to be, material to patentability as defined in § 1.56(b).

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Commissioner for Patents, Washington, D.C. 20231, on August 14, 2001.

Michael Shenker 8-14-01
Attorney for Applicant(s) Date of Signature

Respectfully submitted,

Michael Shenker
Michael Shenker
Attorney for Applicant(s)
Reg. No. 34,250

LAW OFFICES OF
SKJERVEN MORRILL
MacPHERSON LLP
25 METRO DRIVE
SUITE 700
SAN JOSE, CA 95110
(408) 453-9200
FAX (408) 453-7979

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